FIG. 1A

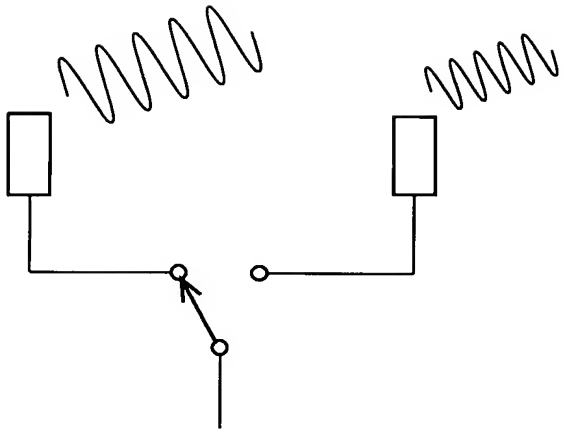


FIG. 1B

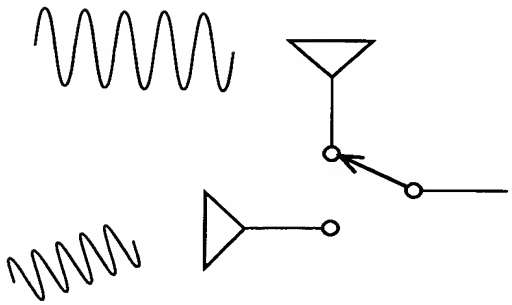


FIG. 1C

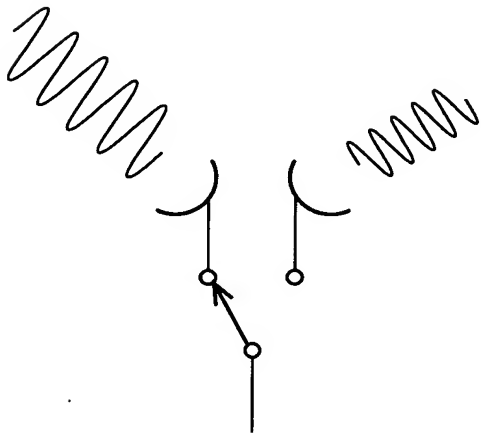


FIG. 2

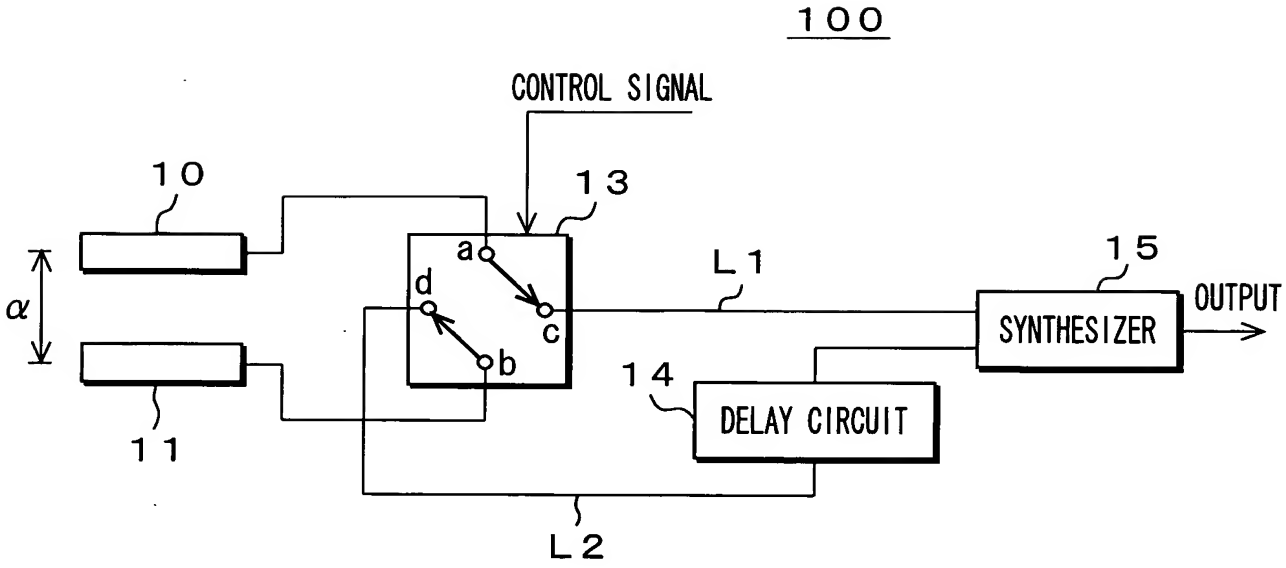

100
CONTROL SIGNAL
10
13
15
L1
OUTPUT
SYNTHESIZER
α
a
d
c
b
14
DELAY CIRCUIT
11
L2

FIG. 3A

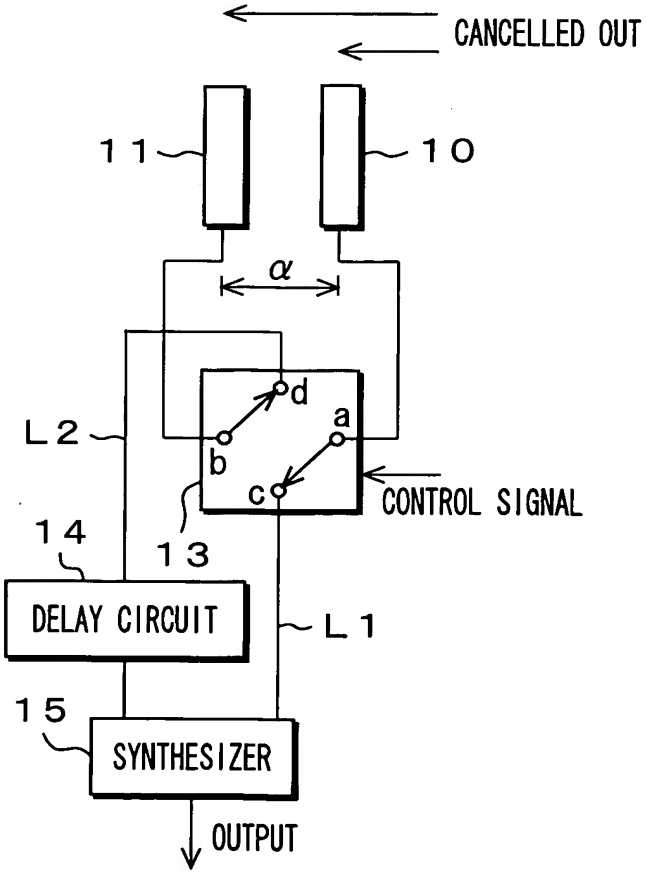

CANCELLED OUT
11
10
α
d
a
L2
b
c
CONTROL SIGNAL
14
13
DELAY CIRCUIT
L1
15
SYNTHESIZER
OUTPUT

FIG. 3B

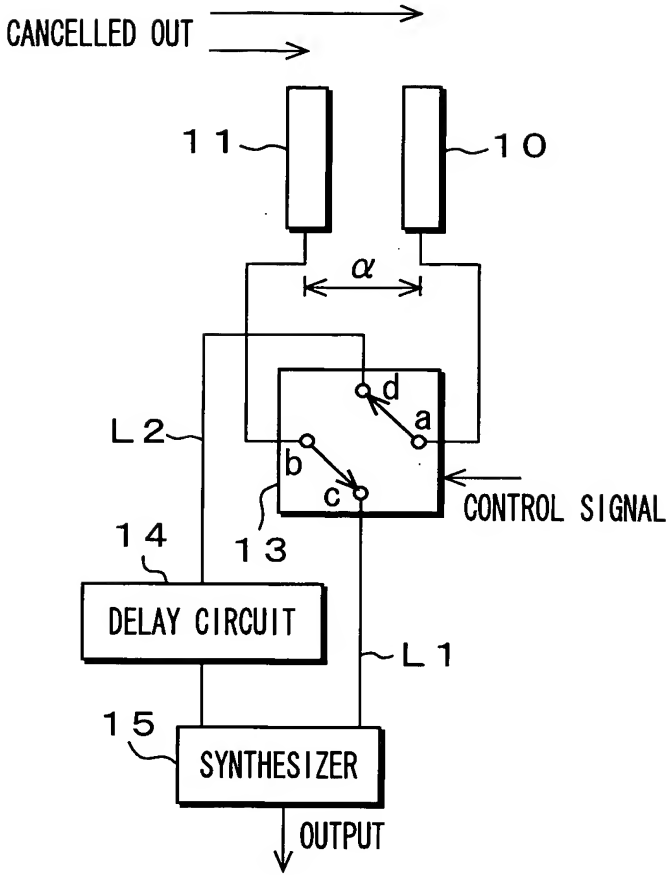

CANCELLED OUT
11
10
α
d
a
L2
b
c
CONTROL SIGNAL
14
13
DELAY CIRCUIT
L1
15
SYNTHESIZER
OUTPUT

FIG. 3C

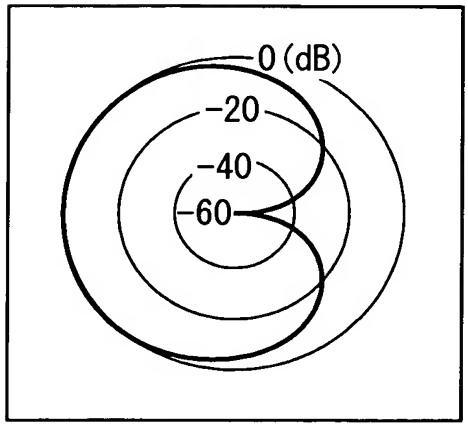

0 (dB)
-20
-40
-60

FIG. 3D

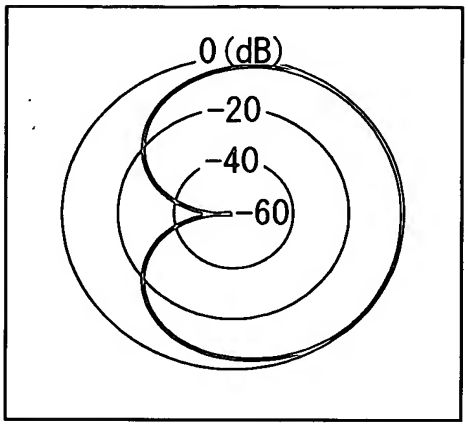


FIG. 4

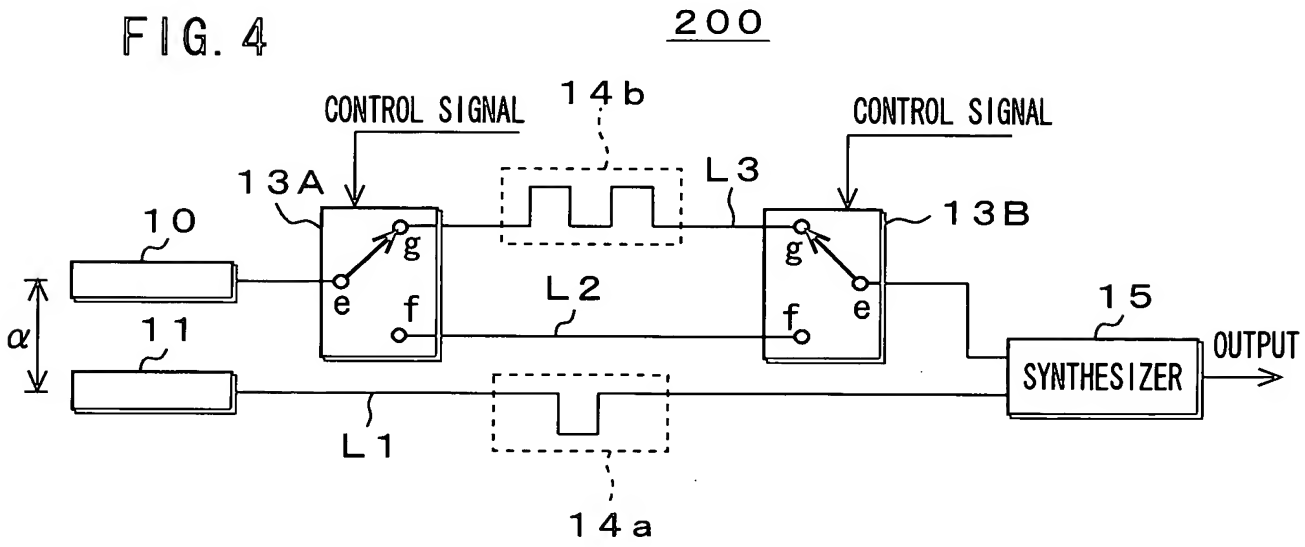


FIG. 5

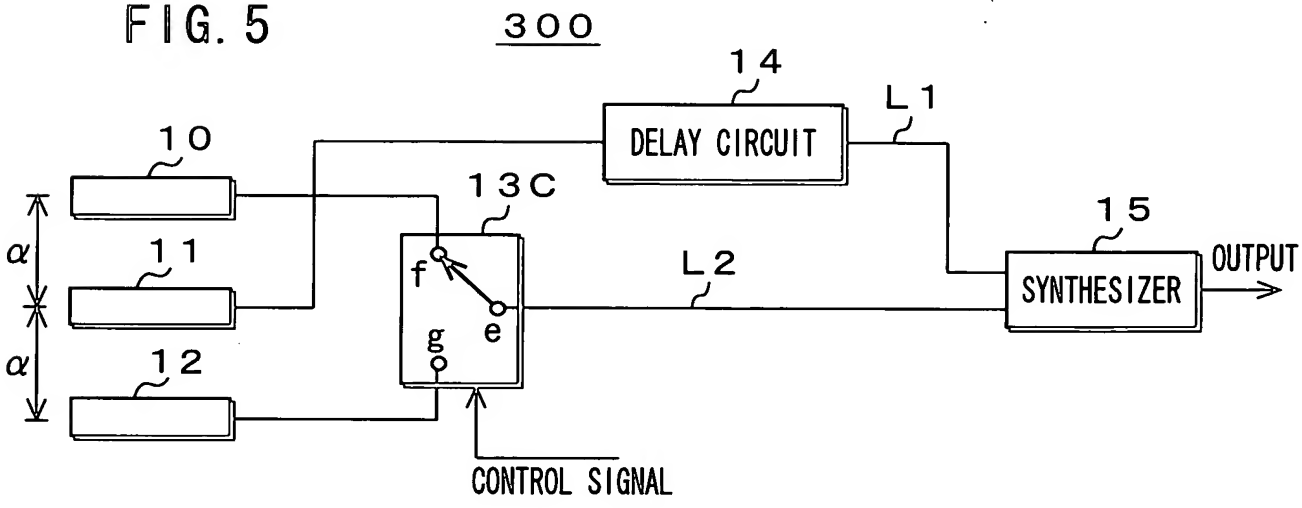
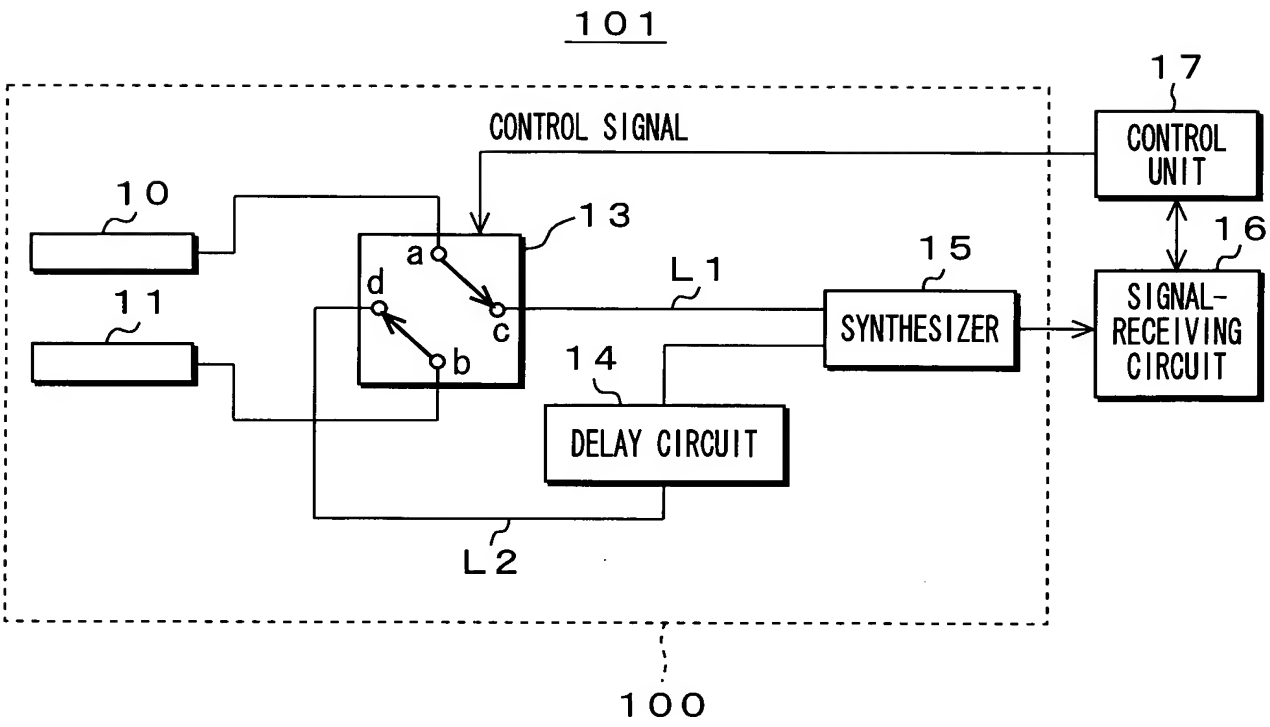


FIG. 6


101
17
CONTROL SIGNAL
CONTROL UNIT
10
13
16
a
d
L1
15
11
c
SIGNAL-RECEIVING CIRCUIT
b
14
SYNTHESIZER
DELAY CIRCUIT
L2
100